A manufacturing method of a semiconductor device according to claim 23 or 24, characterized in that the third conductive layer is a conductive film mainly containing aluminum (Al) or copper (Cu).

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention relates to a semiconductor device having a circuit composed of a thin film transistor (hereinafter referred to as TFT). For example, the invention relates to an electro-optical device represented by a liquid crystal display panel and to electronic equipment mounted with the electro-optical device as a component.

[0002]

In this specification, a 'semiconductor device' refers to a device in general that can function by utilizing semiconductor characteristics, and electro-optical devices, semiconductor circuits, and electronic equipment are semiconductor devices.

[0003]

[Prior Art]

A thin film transistor (hereinafter referred to as TFT) can be formed on a transparent glass substrate, and hence its application to an active matrix liquid crystal display (hereinafter referred to as AM-LCD) has been developed actively. Since a TFT utilizing a crystalline semiconductor film

(typically, a polysilicon film) can provide high mobility, it is considered that it is possible to integrate functional circuits on the same substrate for realizing high definition image display.

[0004]

An active matrix liquid crystal display device requires a million TFTs only for pixels when the resolution of the screen is high definition. When functional circuits are further added, more TFTs become necessary. Each TFT has to have secured reliability and be operated stably in order to realize stable operation of the liquid crystal display device.

[0005]

However, the TFT is considered as not so equal in terms of reliability to a MOSFET that is formed on a single crystal semiconductor substrate. In the TFT, phenomena lowering of mobility and ON current occur when it is operated for a long period of time, as the MOSFET with the same problem. One of causes of the phenomena is characteristic degradation due to hot carriers that accompany increase of a channel electric field.

[0006]

In The MOSFET, on the other hand, the LDD (lightly doped drain) structure is well known as a technique for improving reliability. In this structure, low concentration impurity regions are further provided inside source and drain regions. The low concentration impurity region is called an LDD region. Some TFTs employ the LDD structure.

[0007]

It is another known structure for the MOSFET to make the LDD region somewhat overlap a gate electrode with a gate insulating film sandwiched therebetween. There are several methods for forming this structure. For example, structures called GOLD (Gate-drain overlapped LDD) and LATID (Large-tilt-angle implanted drain) are known. Withstanding against the hot carrier can be enhanced by such structures.

[0008]

There have been attempts to apply these structures of MOSFETs to TFTs. However, application of the GOLD structure (in this specification, a structure having an LDD region to which a gate voltage is applied is called a GOLD structure whereas a structure having only an LDD region to which a gate voltage is not applied is called an LDD structure) to a TFT has a problem that OFF current (current which flows when the TFT is in an OFF state) is larger compared to the LDD structure. Therefore, the GOLD structure is not suitable for a circuit in which OFF current should be as small as possible, such as a pixel matrix circuit of an AM-LCD.

[0009]

[Problems to be solved by the Invention]

An object of the present invention is to provide an AM-LCD having high reliability by form circuits of the AM-LCD of TFTs having suitable structures in accordance with the respective functions of the circuits. The invention aims to accordingly enhance the reliability of a semiconductor device

(electronic equipment) having such AM-LCD.

[0010]

[Means for solving the Problems]

According to a structure of the present invention disclosed in this specification , a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[0011]

In the above structures, the first wiring line may be electrically connected with the second wiring line. That is, a first wiring line and a second wiring line are in the same electric potential, and it becomes possible to add the same voltage to an active layer.

[0012]

According to another structure of the present invention, a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer

is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT; and

the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[0013]

In the above structures, a material with a lower resistance value than the first conductive layer or the second conductive layer is used as the third conductive layer. Concretely, the first conductive layer or the second conductive layer is preferably a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination. And the third wiring line is preferably a conductive film mainly containing aluminum (Al) or copper (Cu).

[0014]

According to another structure of the present invention, a semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT and a storage capacitor, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer,

the active layer includes a low concentration impurity

region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[0015]

In the above structures, the first wiring line may be kept at the ground electric potential or at the source power supply electric potential, or may be kept at the floating electric potential.

[0016]

According to another structure of the present invention, a semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer,

the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[0017]

According to another structure of the present invention, a semiconductor device having a pixel matrix circuit and a driver circuit that are formed on the same substrate,

characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer; and

the first wiring line connected to the pixel TFT is kept at the fixed electric potential or the floating electric potential, and the first wiring connected to the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line connected to the n-channel TFT included in the said driver circuit.

[0018]

In the above structures, the active layer includes a low concentration impurity region that is in contact with the channel formation region and the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[0019]

Further, the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[0020]

According to another structure of the present invention, a manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT

comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TFT, on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer, and

a process of forming a second wiring line on the second insulating layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

[0021]

In the above structures, the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[0022]

According to another structure of the present invention, a manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the

first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TFT, on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer, and

a process of forming a first conductive layer on the second insulating layer,

a process of forming a patterned third conductive layer on the first conductive layer, and

a process of forming a second conductive layer to overlap the third conductive layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

[0023]

[Embodiment Mode of the Invention]

[Embodiment Mode 1]

An embodiment mode of the present invention will be described taking as an example a CMOS circuit (inverter circuit) in which an n-channel TFT (hereinafter referred to as NTFT) is combined with a p-channel TFT (hereinafter referred to as PTFT).

[0024]

A sectional structure thereof is shown in Fig. 1A and a top view thereof is shown in Fig. 1B. The description will be given using symbols which are common to Fig. 1A and Fig.

1B. The sectional views taken along the lines A-A', B-B', and C-C' in Fig. 1B correspond to the sectional views A-A', B-B', and C-C' in Fig. 1A, respectively.

[0025]

In Fig. 1A, 101 denotes a substrate; 102a, 102b, and 102c, first wiring lines; 103, a first insulating layer; 104, an active layer of NTFT; 105, an active layer of PTFT; and 106, a second insulating layer.

[0026]

Thereon, there are a second wiring line 107a laminated as a first conductive layer 107a1 and a second conductive layer 107a2, similarly a second wiring line 107b laminated as a first conductive layer 107b1 and a second conductive layer 107b2, a second wiring line 107c laminated as a first conductive layer 107c1 and a second conductive layer 107c2, and a second wiring line 107d which has a structure of sandwiching a third conductive layer d3 with a first conductive layer 107d1 and a second conductive layer 107d2.

[0027]

108 is a first interlayer insulating layer, 109 to 111 are third wiring lines, 109 and 110 are source wiring lines (including source electrodes), and 111 is a drain wiring line (including a drain electrode).

[0028]

In the CMOS circuit structured as above, a glass substrate, a quartz substrate, a metal substrate, a stainless steel substrate, a plastic substrate, a ceramic substrate,

or a silicon substrate may be used as the substrate 100. When a silicon substrate is used, it is appropriate to oxidize its surface to form a silicon oxide film in advance.

[0029]

Although the first wiring line is a wiring line of the same pattern as shown in Fig. 1B, it is sectioned into 102a, 102b, and 102c for the sake of explanation. Here, the first wiring line 102a represents an intersection with the active layer 103, the first wiring line 102b represents a connection between the TFTs, and the first wiring line 102c represents a power supplying portion which is common to the respective circuits.

[0030]

The first wiring line 102a here functions as a subordinate gate electrode of the NTFT. That is, the electric charge of the channel formation region 112 is controlled by the first wiring line 102a and by the second wiring line (main gate electrode) 107a that is given with the same electric potential as the first wiring line 102a, so that only the first wiring line 102a can apply a gate voltage (or a predetermined voltage) to the LDD regions 113.

[0031]

Accordingly, the GOLD structure is not obtained with only the second wiring line 107a functioning as the gate electrode (the LDD structure is obtained instead), until the first wiring line 102a joins with the second wiring line 107a. Advantages of this structure will be described later. The first wiring

line 102a also functions as a light-shielding layer.

[0032]

Any material can be used for the first wiring line as long as it has conductivity. However, a desirable material is one having heat resistance against the temperature in a later process. For example, a conductive film mainly containing (50% or more composition ratio) an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

[0033]

Given as a feature of this embodiment mode is providing the first wiring line 102a only in the NTFT and not in the PTFT. Although the PTFT in Fig. 1A does not have an offset region or an LDD region either, one of the regions or both of the regions may be formed in the PTFT.

[0034]

With the structure as above, the first wiring line is led from the power supplying portion through the connection to the NTFT to function as a subordinate gate electrode of the NTFT as shown in Fig. 1B.

[0035]

Although the second wiring line is also a wiring line of the same pattern, for the sake of explanation, it is sectioned with almost the same way as the first wiring line is sectioned. In Fig. 1A, 107a represents an intersection with the active layer of the NTFT 104, 107b represents an intersection with

the active layer of the PTFT 105, 107c represents a connection between the TFTs, and 107d represents a power supplying portion.

[0036]

A second wiring line is formed by laminating two kinds of conductive layers basically. Any upper layer and any lower layer can be used as long as it has a conductivity, a tantalum (Ta) film, a titanium (Ti) film, a tungsten (W) film, a molybdenum (Mo) film, and a silicon (Si) film may be used in any combination to form the second wiring lines. An alloy film or silicide film of those may also be used.

[0037]

It is necessary to select materials so as to be possible to pattern to the same form after laminating. That is, the combination, which can make it possible to etch the lower layer side with the upper layer side as a mask, is desirable. And a conductive layer provided as the lower layer must obtain an etching selective ratio to the third conductive layer 107d3.

[0038]

The third conductive layer 107d3 is a conductive film mainly containing aluminum (Al) or copper (Cu),(the component ratio is more than 50%), and the second wiring line is formed by a structure wrapped with the first conductive layer 107d1 and the second conductive layer 107d2 (hereinafter referred to as a cladding structure). This second wiring line 107d forms a wiring line which is corresponding to the power supply portion.

[0039]

The CMOS circuit is an inverter circuit much used as a driver circuit of AM-LCD and other signal process circuits. Since these driver circuit and signal process circuit are integrated in high density, it is desirable to make the width of the wiring line narrow to the utmost. Therefore, the crossing portion (a gate electrode portion) with active layers and the connecting portion (a portion drawing wiring lines) are designed to be as narrow as possible. the lengths of the wiring lines itself in these portion are not so long that it is hardly affected by resistance of the wiring lines.

[0040]

In the power supply portion, however, the length of a wiring line itself is so long that it is much affected by resistance of the wiring line. Therefore, in the present embodiment mode, a material mainly containing aluminum or copper with low resistance is used to reduce resistance of the wiring line. With the structure such as the second wiring line 107d, the width of the wiring line is a little wide, but it is no problem because the power supply portion is formed outside complicatedly integrated circuits.

[0041]

Like an AM-LCD having a diagonal size of 4 inch or less, in the case of applying the present invention to the semiconductor device with wholly small circuits and without extremely long wiring lines, a wiring line to be the power supply portion is also so short that it is unnecessary to use the above-mentioned cladding structure. In other words, it

can be said that the structure as shown in Fig. 1 is effective for an AM-LCD with a diagonal size of 4 inch or more.

[0042]

As described above, the CMOS circuit of this embodiment mode has the two characteristics as follows;

1. The first wiring line (subordinate gate wiring line) is provided only in the NTFT and the same voltage as the second wiring line (main gate wiring line) or a predetermined voltage is applied to the first wiring line, thereby giving the NTFT the GOLD structure.
2. The gate electrode portion and the connecting portion of the second wiring line are made narrow and integrated, and the power supply portion is made to have low resistance with a structure in which the third conductive layer with low resistance is sandwiched with the first and the second conductive layers (the cladding structure).

[0043]

[Embodiment Mode 2]

An embodiment mode of the present invention will be described taking as an example a pixel matrix circuit that uses an NTFT as a pixel TFT. This pixel matrix circuit is formed on the same substrate as the CMOS circuit described in Embodiment Mode 1 at the same time. Therefore, the description in Embodiment Mode 1 may be referred to for details of the wiring lines with the identical names.

[0044]

A sectional structure of the pixel matrix circuit is

shown in Fig. 2A and a top view thereof is shown in Fig. 2B. The description will be given using common symbols to Fig. 2A and Fig. 2B. The sectional views taken along the lines A-A' and B-B' in Fig. 2B correspond to the sectional views A-A' and B-B' in Fig. 2A, respectively

[0045]

In Fig. 2A, 201 denotes a substrate; 202a, 202b and 202c, first wiring lines; 203, a first insulating layer; 204, an active layer of a pixel TFT (NTFT); and 205, a second insulating layer. The pixel TFT shown here as an example has a double gate structure, but a single gate structure or a multi-gate structure in which three or more TFTs are connected in series may be adopted.

[0046]

On the second insulating layer 203, a second wiring line 206a with a structure in which a third conductive layer 206a3 is sandwiched with a first conductive layer 206a1 and a second conductive layer 206a2, a second wiring line 206b laminated as a first conductive layer 206b1 and a second conductive layer 206b2, a second wiring line 206c laminated as a first conductive layer 206c1 and a second conductive layer 206c2, and a capacitor wiring line 207 laminated as a first conductive layer 207a and a second conductive layer 207b.

[0047]

Here, a storage capacitor is formed between the capacitor wiring line 207 and an active layer 204 (namely, a region extended from the drain region) with the first insulating layer 205

as dielectric. In this case, when the first insulating layer 205 is made to have a laminate structure of a silicon nitride and a silicon oxide film provided thereon and a second wiring line is formed after selectively removing the silicon oxide film of the portion to be the storage capacitor, it is realized that the storage capacitor has only a silicon nitride film with high dielectric constant as a dielectric.

[0048]

Denoted by 208 is a first interlayer insulating layer, 209 and 210, third wiring lines, 209, a source wiring line (including a source electrode), and 215, a drain wiring line (including a drain electrode). Formed thereon are a second interlayer insulating layer 211, a black mask 212, a third interlayer insulating layer 213, and a pixel electrode 214.

[0049]

Although the first wiring line is a wiring line of the same pattern as shown in Fig. 2B, it is sectioned into 202a, 202b, and 202c for the sake of explanation. Here, the first wiring line 202a represents a wiring line portion that does not function as a gate electrode, whereas 202b and 202c are intersections with the active layer 204 and function as the gate electrodes.

[0050]

The first wiring lines shown here are formed at the same time when the first wiring lines described in Embodiment Mode 1 are formed. Therefore the material and other explanations thereof are omitted.

[0051]

The first wiring lines 202b and 202c function as light-shielding films of the pixel TFT. In other words, they do not have the function as the subordinate gate wiring line as described in Embodiment Mode 1, and are given a fixed electric potential or set to a floating state (an electrically isolated state). The fixed electric potential may be a ground electric potential or a source power supply electric potential (at the same electric potential as a source wiring line). Then, holes generated by hot carrier injection can be removed from the channel formation regions, and as a result, electric charge is neutralized to disappear hot carrier.

[0052]

Electric charges in the channel formation regions 215 and 216 are thus controlled by the first wiring lines 206b and 206c to provide the LDD structure. Therefore, an increase of OFF current can be contained effectively.

[0053]

The pixel matrix circuit shown in this embodiment mode thus has an NTFT as its pixel TFT, and the structure is the same as the NTFT of the CMOS circuit explained in Embodiment Mode 1. However, the NTFT in the pixel matrix circuit is different from the NTFT in the CMOS circuit in which the GOLD structure is obtained by using the first wiring line as a subordinate gate wiring line through applying a predetermined voltage, since the LDD structure is obtained by giving the first wiring lines a fixed electric potential or setting them

to a floating state in the pixel matrix circuit.

[0054]

In other words, the biggest feature of the present invention is that NTFTs with the same structure are formed on the same substrate and then respectively given the GOLD structure or the LDD structure, with or without being applied a voltage to their first wiring lines (subordinate gate wiring lines). This makes the optimal circuit design possible without increasing the number of manufacture steps.

[0055]

With respect to second wiring lines 206a, 206b and 206c, 206b and 206c are gate electrode portions and 206a is a wiring line portion. Since it is desirable that resistance of the wiring line is lowered as much as possible in the wiring line portion, a cladding structure is adopted. But in the gate electrode portion, since the width of the wiring line decides the length of a channel, it is designed to make the width of lines narrow by laminating the first conductive layer and the second conductive layer.

[0056]

Details and the effect of the cladding structure is explained in Embodiment Mode 1, therefore explanation is omitted here. And as described in Embodiment Mode 1. Needless to say, it is unnecessary that an AM-LCD with a diagonal size of 4 inch or less adopts a cladding structure.

[0057]

The structures of the present invention in the above

will be described in detail in the following embodiments.

[0058]

[Embodiment 1]

In this embodiment, a method of manufacturing the CMOS circuit described in Embodiment Mode 1 will be described. The description will be given with reference to Fig. 3.

[0059]

First, a glass substrate is prepared as a substrate 301, and first wiring lines 302a, 302b, and 302c are formed thereon. The material of the first wiring lines is a laminated film, that a tungsten silicide (WSix) film and a silicon film are laminated in order by sputtering. The order of laminating can of course be reversed and the CVD method can be used as means of depositing. Further, it is effective to form oxide film on the surface after forming the above-mentioned laminated film in the sense of protection of the surface.

[0060]

Other metal films, alloy films, or the like may of course be used as long as the first wiring lines 302a, 302b, and 302c are any film with conductivity. A chromium film or a tantalum film that can be formed into a pattern with a small taper angle is effective in improving the levelness.

[0061]

A second insulating layer 303 of an insulating film containing silicon is formed next. The first insulating layer 303 functions as a gate insulating film in using the first wiring line 302a as a subordinate gate wiring line, as well

as performs as a base film to protect an active layer.

[0062]

This embodiment employs a laminate structure in which a silicon nitride film with a thickness of 50 nm is formed first and a silicon oxide film with a thickness of 80 nm is formed thereon. A silicon oxynitride film expressed as SiO_xN_y (x/y = 0.01 to 100) may be used. In this case, the voltage to withstand thereof can be enhanced by making the nitrogen content larger than the oxygen content.

[0063]

Next, an amorphous silicon film (not shown in the drawing) with a thickness of 50 nm is formed and a crystalline silicon film is formed by crystallizing using a known laser crystallization technique. And the crystalline silicon film is patterned to form active layers 304 and 305. In the process of crystallization in this embodiment, an amorphous silicon film is irradiated by processing the pulse-oscillating type KrF excimer laser light into a linear beam.

[0064]

Although this embodiment uses as a semiconductor film for the active layers a crystalline silicon film obtained by crystallizing an amorphous silicon film, other semiconductor films such as a microcrystalline silicon film may be used or a crystalline silicon film may be deposited directly. A compound semiconductor film such as a silicon germanium film may be used except silicon films.

[0065]

A second insulating layer 306 is formed next of a silicon oxide film, a silicon oxynitride film, or a silicon nitride film, or a laminate film of those so as to cover the active layers 304 and 305. A silicon oxynitride film is formed here by plasma CVD to a thickness of 100 nm. The second insulating layer functions as a gate insulating film when the second wiring line is used as a main gate wiring line.

[0066]

Next, a tantalum film 307 with a thickness of 20 nm is formed as a first conductive layer, and a third conductive layer 308 of an aluminum film to which scandium is added, is formed thereon. And a second conductive layer 309 of a tantalum film is formed to have a thickness of 200 nm. Either sputtering or CVD can be used to form these films.

[0067]

After the state of Fig. 3A is thus obtained, resist masks 310 and 311 are formed to etch the first conductive layer 307 and the second conductive layer 309. In this way, a second wiring line 312 is formed of the laminate structure of the tantalum films. The second wiring line 312 corresponds to the second wiring line (main gate wiring line) 107a in Fig. 1A. [0068]

Next, an element which belongs to Group 15 (typically, phosphorus or arsenic)is doped to form low concentration impurity regions 313. A channel formation region of the NTFT is defined simultaneously. In this embodiment, phosphorus is used as the element which belongs to Group 15, and ion doping

method that does not perform mass separation is employed. (Fig. 3B)

[0069]

Doping conditions include setting the acceleration voltage to 90 keV, and adjusting the dose so that phosphorus is contained in a concentration of 1×10^{16} to 1×10^{19} atoms/cm^3 (preferably 5×10^{17} to 5×10^{18} atoms/cm^3). This concentration later becomes the impurity concentration in the LDD regions, and hence is needed to be controlled precisely.

[0070]

The resist masks 310 and 311 are then removed and resist masks 315 to 318 are newly formed. The first conductive layer 307 and the second conductive layer 309 are etched to form second wiring lines 319 to 321. The second wiring lines 319, 320 and 321 respectively correspond to the second wiring lines 107b, 107c and 107d of Fig. 1A.

[0071]

Next, an element which belongs to Group 13 (typically boron or gallium) is doped to form an impurity region 322. At this time, a channel formation region 323 of the PTFT is defined simultaneously. In this embodiment, boron is used as the element which belongs to Group 13, and ion doping method that does not perform mass separation is employed. (Fig. 3C)

[0072]

Doping conditions include setting the acceleration voltage to 75 keV, and adjusting the dose so that boron is contained in a concentration of 1×10^{19} to 5×10^{21} atoms/cm^3

(preferably 1 x 10^{20} to 1 x 10^{21} atoms/cm^3).

[0073]

The resist masks 315 to 318 are then removed and resist masks 324 to 327 are formed again. In this embodiment, the resist masks are formed by using a back side exposure method. For the resist masks 324, 326 and 327, the first wiring lines serve as masks whereas the second wiring lines serve as masks for the resist mask 325. With the first wiring lines as masks, a small amount of light reaches behind the wiring lines and hence the line width in this case is narrower than the width of the first wiring lines. The line width can be controlled by exposure conditions.

[0074]

The resist masks can of course be formed by using masks instead. In this case, the degree of freedom in pattern design is raised but the number of masks is increased.

[0075]

After the resist masks 324 to 327 are thus formed, a step of doping an element which belongs to Group 15 (phosphorus in this embodiment) is conducted. Here, the acceleration voltage is set to 90 keV, and the dose is adjusted so that phosphorus is contained in a concentration of 1 x 10^{19} to 5 x 10^{21} atoms/cm^3 (preferably 1 x 10^{20} to 1 x 10^{21} atoms/cm^3).

[0076]

Through this step, a source region 328, a drain region 329 and LDD regions 330 of the NTFT are defined. Further, a source region 331 and a drain region 332 of the PTFT are

defined. A source region and a drain region of the PTFT are also doped with phosphorus in this step. However, the P type conductivity thereof can be maintained without reversing to the N type conductivity if they are doped with boron in a higher concentration in the previous step.

[0077]

After the NTFT and the PTFT are thus doped with impurity elements each imparting one of the conductivity types, the impurity elements are activated by furnace annealing, laser annealing, or lamp annealing, or by using these annealing methods in combination.

[0078]

The state of Fig. 3D is obtained in this way. Then a first interlayer insulating layer 333 is formed of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a resin film, or a laminate film of those films. Contact holes are opened to form source wiring lines 334 and 335 and a drain wiring line 336. (Fig. 3E).

[0079]

The first interlayer insulating layer 333 in this embodiment has a two-layered structure in which a silicon nitride film with a thickness of 50 nm is formed first and a silicon oxide film with a thickness of 950 nm is formed thereon. The source wiring lines and the drain wiring line in this embodiment are formed by patterning a three-layered laminate structure obtained by successively forming, by sputtering, a titanium film with a thickness of 100 nm, an aluminum film containing

titanium and having a thickness of 300 nm, and another titanium film with a thickness of 150 nm.

[0080]

A CMOS circuit with a structure as shown in Fig. 3E is thus completed. The CMOS circuit of this embodiment has the structure shown in Fig. 1A, and the explanation thereof is omitted here because it is described in detail in Embodiment Mode 1. To obtain the structure of Fig. 1A, the manufacturing process is not necessarily limited to this embodiment. For example, the NTFT may take the double gate structure while the PTFT is given the single gate structure.

[0081]

The CMOS circuit described in this embodiment serves as a basic unit circuit for constructing a driver (driving) circuit (including a shift register circuit, a buffer circuit, a level shifter circuit, a sampling circuit, etc.) and other signal processing circuits (such as a divider circuit, a D/A converter circuit, a γ correction circuit, and an operation amplifier circuit) in an AM-LCD.

[0082]

In this embodiment, the first wiring line of the NTFT is used as a subordinate gate wiring line to thereby obtain a substantial GOLD structure and prevent degradation due to hot carrier injection. Accordingly, a circuit with a very high reliability can be formed.

[0083]

By narrowing the width of wiring lines in a part with

high integration and by using a cladding structure in a part (an electric power supplying portion) which does not have so high integration, The structure, in which resistance of wiring lines is reduced and the delayed time because of resistance of wiring lines are reduced, is realized.

[0084]

[Embodiment 2]

In this embodiment, a method of manufacturing the pixel matrix circuit described in Embodiment Mode 2 will be described. The description will be given with reference to Figs. 4 and 5. The pixel matrix circuit is formed on the same substrate as the CMOS circuit shown in Embodiment 1 at the same time. Therefore, the description will be given in relation to the manufacturing process of Embodiment 1 and the same symbols as those in Fig. 3 are used when necessary.

[0085]

First, second wiring lines 401a, 401b, and 401c are formed on the glass substrate 301. The second wiring lines have the material as described in Embodiment 1. Next, the first insulating layer 303, an active layer of a pixel TFT 402, the second insulating layer 306, the first conductive layer 307, a third conductive layer 403 and the second conductive layer 309 are formed consulting Embodiment 1. Thus obtained is the state of Fig. 4A. The CMOS circuit being formed simultaneously is now in the state of Fig. 3A.

[0086]

Next, resist masks 404 to 407 are formed to etch the

first conductive layer 307 and the second conductive layer 309. Second wiring lines 408 and 409 and a capacitor wiring line 410 are thus formed. The second wiring line 408 corresponds to the second wiring line 206b in Fig. 2A and the second wiring line 409 corresponds to the second wiring line 206c in Fig. 2A. Further, the capacitor wiring line 410 corresponds to the capacitor wiring line 207 in Fig. 2A.

[0087]

The phosphorus doping step for forming LDD regions later is conducted next to form low concentration impurity regions 411 to 413. Channel formation regions 414 and 415 are defined simultaneously. This step corresponds to the step of Fig. 3B. Accordingly, the material and thickness of the second wiring lines and phosphorus doping conditions in the step of Fig. 4B are the same as Embodiment 1.

[0088]

A step which is corresponding to the step of Fig. 3C is conducted next. First, resist masks 416 and 417 are formed to etch the first conductive layer 307 and the second conductive layer 309, and thus a second wiring line 418 is formed. This second wiring line 418 corresponds to the second wiring line 206a in Fig. 2A.

[0089]

Next, the boron doping step for forming the PTFT of the CMOS circuit is conducted. In this Embodiment, the pixel matrix circuit is entirely covered with a resist mask 417 because a pixel TFT is formed of NTFT. (Fig. 4C)

[0090]

After the resist mask 416 and 417 are then removed, resist masks 419 to 422 are formed by the back side exposure method. Then the phosphorus doping step is conducted to form a source region 423, a drain region 424 and a LDD region 425. The conditions of the back side exposure and phosphorus doping may be set in accordance with the step of Fig. 3D in Embodiment 1.

[0091]

The source region and the drain region in Fig. 4D are named so for the sake of explanation. However, a source region and drain region in a pixel TFT are reversed between charging and discharging and hence there is no definite discrimination between the two regions.

[0092]

After the doping steps of phosphorus and boron are finished, the impurity elements are activated as in Embodiment 1. Then the first interlayer insulating film 333 is formed and contact holes are formed therein to form a source wiring line 426 and a drain wiring line 427. The state of Fig. 4E is thus obtained. The CMOS circuit at this point is in the state of Fig. 3E.

[0093]

Next, a second interlayer insulating layer 428 is formed to cover the source wiring line 426 and the drain wiring line 427. In this embodiment, a silicon nitride film with a thickness of 30 nm is formed as a passivation film and an acrylic film

with a thickness of 700 nm is formed thereon. Of course, an insulating film mainly containing silicon such as a silicon oxide film, or other resin films may be used. Other resin films that are usable are a polyimide film, a polyamide film, a BCB (benzocyclobutene) film, and the like.

[0094]

Next, a black mask 429 is formed of a titanium film with a thickness of 100 nm. Other films may be used to form the black mask 427 if they have light-shielding property. Typically, a chromium film, an aluminum film, a tantalum film, a tungsten film, a molybdenum film, a titanium film, or a laminate of these films is used.

[0095]

A third interlayer insulating layer 430 is then formed. Though an acrylic film with a thickness of 1 μm is used in this embodiment, the same material as the second interlayer insulating layer may be used instead.

[0096]

A contact hole is next formed in the third interlayer insulating layer 430 to form a pixel electrode 431 of a transparent conductive film (typically an ITO film). The pixel electrode 431 is electrically connected to the drain wiring line 427. Since the contact hole accordingly has to be very deep, and hence it is effective in preventing failure such as break of the pixel electrode to form the contact hole with its inner wall tapered or curved.

[0097]

A pixel matrix circuit with a structure as shown in Fig. 5A is thus completed. Although the example shown in this embodiment is an example of manufacturing a transmission type AM-LCD using a transparent conductive film as a pixel electrode, a reflection type AM-LCD can readily be manufactured when a metal film with high reflectance (such as a metal film mainly containing aluminum) is used as the pixel electrode.

[0098]

The substrate in the state of Fig. 5A is called an active matrix substrate. This embodiment also describes a structure in the case of actually manufacturing an AM-LCD.

[0099]

After the state of Fig. 5A is obtained, an orientation film 432 with a thickness of 80 nm is formed. An opposite substrate is fabricated next. The opposite substrate prepared is a glass substrate 433 on which a color filter 434, a transparent electrode (opposite electrode) 435, and an orientation film 436 are formed. The orientation films 432 and 435 are subjected to rubbing treatment, and the active matrix substrate is bonded to the opposite substrate using a seal (sealing member). Then a liquid crystal 436 is held therebetween. A spacer for maintaining the cell gap may be provided if necessary.

[0100]

An AM-LCD with a structure as shown in Fig. 5B (the part of a pixel matrix circuit) is thus completed. The second interlayer insulating layer 428 and the third interlayer insulating layer 430 of this embodiment is also formed over

the CMOS circuit shown in Embodiment 1 in actuality. When the black mask 429 and the pixel electrode 431 are formed, wiring lines may be formed, at the same time, of the same materials that constitute the black mask and the pixel electrode, and the wiring lines may be used as lead out wiring lines (fourth wiring lines or fifth wiring lines) of a driver circuit and signal processing circuit of the AM-LCD.

[0101]

In this embodiment, the first wiring lines 401b and 401c provided in the pixel TFT are set to the fixed electric potential (the ground electric potential or the source electric potential). This makes it possible to draw holes generated in the drain end due to hot carrier injection to the first wiring lines, thereby improving the reliability. Although the first wiring lines 401b and 401c may of course be set to a floating state, the hole drawing effect cannot be expected in this case.

[0102]

As shown in the top view of Fig. 2B, the second wiring line 418 deposited in the wiring line portion adopts the cladding structure to reduce resistance of wiring lines as much as possible.

[0103]

[Embodiment 3]

In this embodiment, an AM-LCD is provided with a pixel matrix circuit and a CMOS circuit (concretely, a driver circuit and signal processing circuit constructed of CMOS circuits)

according to the present invention, and the appearance thereof is shown in Fig. 6.

[0104]

On an active matrix substrate 601, a pixel matrix circuit 602, a signal line driving circuit (source driver circuit) 603, scanning line driving circuits (gate driver circuits) 604, and a signal processing circuit (including a signal divider circuit, a D/A converter circuit, and a γ correction circuit) 605 are formed, and an FPC (flexible printed circuit) 606 is attached. Denoted by 607 is an opposite substrate.

[0105]

The various circuits formed on the active matrix substrate 601 are illustrated in detail in a block diagram of Fig. 7.

[0106]

In Fig. 7, 701 denotes a pixel matrix circuit that functions as an image display unit. 702a, 702b, and 702c represent a shift register circuit, a level shifter circuit, and a buffer circuit, respectively. The three together constitute a gate driver circuit.

[0107]

In the block diagram of the AM-LCD in Fig. 7, the gate driver circuits are provided to sandwich a pixel matrix circuit and to share the same gate wiring lines. This is, application of voltage to the gate wiring lines is still possible even after one of the gate drivers has failure occurred, thereby giving the AM-LCD redundancy.

[0108]

703a, 703b, 703c, and 703d represent a shift register circuit, a level shifter circuit, a buffer circuit, and a sampling circuit, respectively. The four together constitute a source driver circuit. A precharge circuit 14 is provided at the opposite side of the source driver circuit across the pixel matrix circuit.

[0109]

The reliability of an AM-LCD having circuits as shown in Fig. 6 can be greatly improved by employing the present invention. In this case, CMOS circuits which form a driver circuit and a signal processing circuit are made in accordance with Embodiment 1 and a pixel matrix circuit is made in accordance with Embodiment 2.

[0110]

[Embodiment 4]

This embodiment gives a description on a case where a CMOS circuit is structured differently from Embodiment 1 and a pixel matrix circuit is structured differently from Embodiment 2. To be specific, circuits are given different structures in accordance with the specifications the circuits demand.

[0111]

The basic structure of the CMOS circuit is the structure shown in Fig. 1A and the basic structure of the pixel matrix circuit is the structure shown in Fig. 2A. Therefore only the part that needs explanation is denoted by a symbol and

explained in this embodiment.

[0112]

The structure shown in Fig. 8A lacks an LDD region at the source side of the NTFT and has an LDD region 801 only at the drain side. The CMOS circuit, which is used for a driver circuit and a signal processing circuit, is required to operate at high speed and hence resist components that can cause reduction in operation speed have to be removed as much as possible.

[0113]

In the case of the CMOS circuit according to the present invention, a gate voltage is applied to a first wiring line which functions as a subordinate gate wiring line to obtain the GOLD structure and prevent degradation due to hot carrier injection. However, it is sufficient that an LDD region that is overlapped with a gate electrode is formed at an end of a channel formation region at the drain region side where hot carriers are injected.

[0114]

Accordingly, an LDD region at an end of the channel formation region at the source region side is not indispensable. On the contrary, the LDD region provided at the source region side might work as a resist component. The structure as Fig. 8A is therefore effective in improving the operation speed.

[0115]

The structure of Fig. 8A cannot be applied to a circuit that behaves like a pixel TFT in which a source region and a drain region are switched. Since a source region and a drain

region of a CMOS circuit are normally fixed, the structure such as Fig. 8A can be realized.

[0116]

Fig. 8B is basically the same as Fig. 8A, but the width of an LDD region 802 in Fig. 8B is narrower than in Fig. 8A. Specifically, the width is set to 0.05 to 0.5 μm (preferably 0.1 to 0.3 μm). The structure in Fig. 8B is capable of not only reducing the resist component at the source region side but also reducing the resist component at the drain region side as much as possible.

[0117]

This structure is actually suitable for a circuit that is driven at as low voltage as 3 to 5 V and is required to operate at high speed, such as a shift register circuit. Since the operation voltage is low, the narrow LDD region (LDD region that is overlapped with a gate electrode, strictly speaking) does not raise the problem of hot carrier injection.

[0118]

Of course, LDD regions in the NTFT may be completely omitted in some cases if the omission is limited to the shift register circuit. In this case, the NTFT of the shift register circuit has no LDD region while other circuits in the same driver circuit employ the structure shown in Fig. 1A or the structure shown in Fig. 8B.

[0119]

Next, Fig. 8C shows an example of a CMOS circuit in which its NTFT has the double gate structure and PTFT has the

single gate structure. In this case, LDD regions 805 and 806 are provided only at ends of channel formation regions 803 and 804 which are closer to drain regions.

[0120]

The width of an LDD region is determined by the amount of light that reaches around in the back side exposure step, as shown in Fig. 3D. However, if resist masks are formed by mask alignment, the masks can be designed freely. Forming an LDD region only at one side is easy also in the structure shown in Fig. 8C if a mask is used.

[0121]

However, forming an LDD region only at one side by the back side exposure method is possible when gate wiring lines (second wiring lines) 807a and 807b are formed so as to be shifted from first wiring lines 808 and 809 as in this embodiment.

[0122]

This structure eliminates the resist component due to an LDD region at the source side, and the double gate structure has an effect of diffusing and easing the electric field applied between the source and the drain.

[0123]

The structure in Fig. 8D is a mode of a pixel matrix circuit. In the structure of Fig. 8D, LDD regions 809 and 810 are provided at either the side closer to the source region or the side closer to the drain region. In other words, no LDD region is provided between two channel formation regions

811 and 812.

[0124]

In the case of a pixel TFT, a source region and a drain region are frequently switched since charging and discharging are repeated. Accordingly, when the pixel TFT has a structure of Fig. 8D, the LDD region is always provided at the drain region side of the channel formation region whichever region serves as the drain region. On the other hand, it is effective in increasing ON current (current flowing when the TFT is in an ON state) to omit an LDD region to be a resist component since there is no electric field concentration between the channel formation regions811 and 812.

[0125]

An LDD region is not provided at an end of the channel formation region at the source region side in the structures of Figs. 8A to 8D. However, the LDD region may be provided there if it has a narrow width. This structure may be obtained by forming resist masks through mask alignment or by the back side exposure method after the positions of the first wiring lines and the second wiring lines are adjusted.

[0126]

Needless to say, the structure of this embodiment can be combined with Embodiments 1 and 2, and applied to the AM-LCD shown in Embodiment 3.

[0127]

[Embodiment 5]

This embodiment shows, with reference to Fig. 9, a

case of forming a storage capacitor with a different structure from the pixel matrix circuit shown in Embodiment 2. Since the fundamental structure is the same as Fig. 2A, only necessary parts are denoted by the symbols in this embodiment and explained.

[0128]

In the structure shown in Fig. 9A, a storage capacitor is formed of a capacitor wiring line 901 which is formed in the same layer as the first wiring line, a first insulating layer 902, and an active layer 903(strictly speaking, the portion extended from a drain region).

[0129]

This structure has the advantage of having conductivity since an element which belongs to Group 13 or 15 is doped at high concentration into a portion of the active layer which functions as an electrode of the storage capacitor. The element which belongs to Group 13 or 15 may of course be formed at the same time as the process of forming a source region or a drain region.

[0130]

In the case of the structure described in "Embodiment Mode 2", the active layer which functions as the electrode of the storage capacitor is not doped with the impurity element which give a conductivity because the second wiring line performs a mask, the state that an inverse layer is formed in the active layer by applying a voltage to the capacitor wiring line at all times, must be kept. In the structure of Fig. 9A, however, the active layer itself which functions as the electrode of

the storage capacitor has a conductivity, and it is not necessary to apply voltage and what has to be done is only fixing in the ground electric potential.

[0131]

Thus, it can be said that it is an effective structure to lower power consumption because it is unnecessary that the extra voltage is applied.

[0132]

The structure of Fig. 9B is an example of combining the structure of the storage capacitor shown in Fig. 2A with the structure of the storage capacitor shown in Fig. 9A. Concretely, a first storage capacitor is formed of a first capacitor wiring line 904 which is in the same layer as the first wiring line, a first insulating layer 905 and an active layer 906, and a second storage capacitor is formed of the active layer 906, a second insulating layer 907 and a second capacitor wiring line 908 which is in the same layer as the first wiring line.

[0133]

This structure can ensure a nearly double capacitor of the structure of the storage capacitor shown in Fig. 2A and Fig. 9A without increasing the number of process. Specially, the AM-LCD with higher definition requires the storage capacitor with a smaller surface area in order to improve the aperture ratio. In such a case, the structure of Fig. 9B is effective.

[0134]

It is effective to use the structure of this embodiment

in AM-LCD shown in Embodiment 3.

[0135]

[Embodiment 6]

This embodiment shows, with reference to Fig. 10, an example of a case in which the first conductive layer that consists of the second wiring line is omitted in the CMOS circuit shown in Fig. 1A and in the pixel matrix circuit shown in Fig. 2A. In Fig. 10A, the same structures as Fig. 1A or Fig. 2A are denoted by the same symbols.

[0136]

In the CMOS circuit of Fig. 10A, all of second wiring lines 11 to 13 are formed of a tantalum film with a single layer, that is, are a structure having the first conductive layer omitted and having the second wiring line formed of only the second conductive layer, compared with the structure of Fig. 1A. The thickness is 200 to 400 nm. Except tantalum, a conductive film mainly containing an element selected from the group consisting of titanium, tungsten, molybdenum, and silicon, or an alloy film or silicide film containing the above elements in combination may of course be used.

[0137]

In the case of this structure, the power supply portion (the portion denoted as the cladding structure in Fig. 1A) of the second wiring line has a structure in which the third conductive layer 14a is covered by the second conductive layer 14b. Undesirably, this structure might allow aluminum or copper that is an element constituting the third conductive layer

14a to diffuse into a second insulating layer 106. Therefore, when a silicon nitride film is formed on the surface of the second insulating layer 106, it is possible to prevent diffusion of aluminum or copper effectively.

[0138]

The structure of this embodiment may also be applied to a pixel matrix circuit. The pixel matrix circuit in Fig. 10B uses only a second conductive layer (a tantalum film in this embodiment) for a second wiring line (a gate wiring line) 16 and 17 and a capacitor wiring line, and employs the structure in which a third conductive layer 15a is covered with a second conductive layer 15b for a part of the gate wiring line that is required to reduce wiring line resistance.

[0139]

Needless to say, the circuits shown in Fig. 10A and Fig. 10B are both formed on the same substrate at the same time.

[0140]

The structure of this embodiment can be realized only by omitting a process of forming the first conductive layer in the manufacturing process shown in Embodiment 1 and Embodiment 2. It can also be applied to the AM-LCD of Embodiment 3 and can be combined with the structure shown in Embodiment 4 and 5.

[0141]

[Embodiment 7]

This embodiment shows, with reference to Fig. 11, an

example of a case in which the gate electrode portion of the NTFT has a cladding structure in the CMOS circuit shown in Fig. 1A and in the pixel matrix circuit shown in Fig. 2A. In Fig. 11A, the same structures as Fig. 1A or Fig. 2A are denoted by the same symbols.

[0142]

In the CMOS circuit shown in Fig. 11A, the gate electrode 21 of the NTFT has a cladding structure in which a third conductive layer 21c is wrapped with a first conductive layer 21a and a second conductive layer 21b. The length of a channel formation region 22 is coincident with the line width of a third conductive layer 21c.

[0143]

The LDD region 23 can be substantially divided into two regions. One is overlapped with a gate electrode 21 which is a portion of the second wiring line, the other is not overlapped with the gate electrode 21. In the structure of this embodiment, the GOLD structure is realized only with a gate electrode which is a portion of the second wiring line. Since the LDD region which is not overlapped with a gate electrode is provided outside the LDD region which is overlapped with a gate electrode, OFF current can be made much smaller.

[0144]

Similarly, in the pixel matrix circuit shown in Fig. 11B, both gate electrodes 24 and 25 of the pixel TFT adopts the cladding structure in which third conductive layers 24c and 25c are respectively wrapped with first conductive layers

24a and 25a and second conductive layers 24b and 25b. The lengths of channel formation regions 26 and 27 are coincident with the widths of lines of third conductive layers 24c and 25c, respectively. Both the LDD regions 28 and 29 can be substantially divided into two regions in the same way as the LDD region 23.

[0145]

In the case of the structures shown in "Embodiment Mode 1" and "Embodiment Mode 2", the GOLD structure is realized by adding a gate voltage to the first wiring lines (subordinate gate wiring lines) in the CMOS circuit while the LDD structure is adopted to reduce OFF current in the pixel matrix circuit in order to avoid increase in OFF current which is a disadvantage of the GOLD structure. Therefore, the advantage of the GOLD structure which prevents degradation of ON current can not be obtained.

[0146]

In this embodiment, however, even in the pixel matrix circuit, the NTFT with the GOLD structure is realized, and it can be possible to improve the reliability more. Of course, it is the very reason for the pixel TFT with the GOLD structure to provide the LDD region which is not overlapped with a gate electrode outside the LDD region which is overlapped with the gate electrode.

[0147]

Here, a description is given, with reference to Fig. 12, on the manufacturing process to realize the structure of

this embodiment. Since it is fundamentally same as the process described in Embodiment 1, the new symbols are used only when necessary.

[0148]

First, a third conductive layer 308 is formed in accordance with the process of Embodiment 1. In the case of this embodiment, a third conductive layer 31 on the NTFT at the same time as when the third conductive layer 308 is formed. Then, a resist mask 32 is formed and the phosphorus doping step is conducted. With respect to the doping condition, the process of Fig. 3B in Embodiment 1 may be referred to. Through this step, the low concentration impurity regions 33 and 34 are formed and the channel formation region 35 is defined. (Fig. 12A)

[0149]

After the resist mask 32 is removed, second conductive layers 36 and 37 are formed. Through this step, a main gate wiring line of NTFT 38 is formed. (Fig. 12B)

[0150]

Next, resist masks 315 to 318 are formed, and then the boron doping step is conducted. With the doping condition, the process of Fig. 3C in Embodiment 1 may be referred to. Thus, after the phosphorus doping step and the boron doping step are conducted, the doped impurity element is activated in the same way as Embodiment 1 to obtain the state of Fig. 12C.

[0151]

Next, after the resist masks 315 to 318 are removed, the back side exposure method is used to form resist masks 324 to 327, and the phosphorus doping step is then conducted. With respect to the doping conditions, the process of Fig. 3D in Embodiment 1 may be referred to.

[0152]

Through this step, a source region 39, a drain region 40 and low concentration impurity regions (the LDD regions) 41 of the NTFT are formed. (Fig. 12D)

[0153]

At this time, the length of the portion of the LLD region 41 with which the gate electrode 38 is overlapped, is set to 0.1 to 3.5 μm (typically 0.1 to 0.5 μm, preferably 0.1 to 0.3 μm) whereas the length of the portion with which the gate electrode 38 is not overlapped, is set to 0.5 to 3.5 μm (typically 1.5 to 2.5 μm).

[0154]

Thereafter, a CMOS circuit with such a structure as shown in Fig. 11A is completed by forming the first interlayer insulating layer 108, the source wiring lines 109 and 110 and the drain wiring line 111, through the same step as Embodiment 1.

[0155]

Although he description in this embodiment takes as an example the manufacturing step of a CMOS circuit, the structure of Fig. 11B may be obtained through the similar manufacturing

[0161]

In Fig. 13, the LDD region 51 can be substantially divided into two portions in which one is overlapped and the other is not overlapped with a first wiring line 102a. Therefore, when a gate voltage is applied to the first wiring line 102a, the structure of the NTFT of Fig. 13 has the LDD region which is not overlapped with a gate electrode outside the LDD region which is overlapped with a gate electrode.

[0162]

As described in Embodiment 8, this structure has an effect that degradation of ON current is prevented, which is the advantage of the GOLD structure, and obtains electrical characteristics that increase of OFF current, which is the defect of the GOLD structure, is suppressed. Accordingly, a CMOS circuit with very high reliability can be realized.

[0163]

Here, although an example of a CMOS circuit is described, the structure of this embodiment may be applied to a pixel matrix circuit.

[0164]

To realize the structure of this embodiment, the back side exposure method may not be used in the process shown in Fig. 3D in Embodiment 1. That is, the structure of this embodiment can be readily obtained by performing a step of doping phosphorus after providing the wider resist masks than the first wiring line with usual mask alignment.

[0165]

With respect to the lengths of the LDD region (the lengths of the portion that is overlapped and the portion that is not overlapped with a gate electrode), the range shown in Embodiment 8 may be referred to.

[0166]

The structure of this embodiment can also be applied to the AM-LCD of Embodiment 3 and can be freely combined with the structure shown in Embodiments 4 to 7.

[0167]

[Embodiment 10]

This embodiment describes a case in which other methods except laser crystallization is used to form the active layer shown in Embodiment 1 or 2

[0168]

Specifically, a case is described in which a crystalline semiconductor film used as an active layer is formed by the thermal crystallization method using a catalytic element. In the case of using the catalytic element, it is desirable to use the technique disclosed in Japanese Patent Application Laid-open No. Hei 7-130652 (corresponding to US. Patent Application No. 08/329,644 or US. Patent Application No. 08/430,623) and Japanese Patent Application Laid-open No. Hei 8-78329. Specially, it is preferable to use nickel as the catalytic element.

[0169]

The structure of this embodiment can be combined freely with all of the structures of Embodiments 1 through 9.

[0170]

[Embodiment 11]

This embodiment describes a case, as a method of forming an active layer, in which the thermal crystallization method shown in Embodiment 10 is used and the catalytic element used is removed from the crystalline semiconductor film. To remove the catalytic element, this embodiment employs the technique disclosed in Japanese Patent Application Laid-open No. Hei 10-135468 (corresponding to US. Patent Application No. 08/951,193) or Japanese Patent Application Laid-open No. Hei 10-135469 (corresponding to US. Patent Application No. 08/951,819).

[0171]

It is the technique described in the publication to remove a catalytic element used in crystallization of an amorphous semiconductor film by utilizing gettering effect of halogen after the crystallization. With this technique, the concentration of the catalytic element in the crystalline semiconductor film can be reduced to 1×10^{17} atoms/cm^3 or less, preferably to 1×10^{16} atoms/cm^3.

[0172]

The structure of this embodiment can be combined freely with all of the structures of Embodiments 1 through 10.

[0173]

[Embodiment 12]

This embodiment describes a case, as a method of forming an active layer, in which the thermal crystallization method

shown in Embodiment 10 is used and the catalytic element used is removed from the crystalline semiconductor film. To remove the catalytic element, this embodiment employs the technique disclosed in Japanese Patent Application Laid-open No. Hei 10-270363 (corresponding to US. Patent Application No. 09/050,182).

[0174]

It is the technique described in the publication to remove a catalytic element used in crystallization of an amorphous semiconductor film by utilizing the gettering effect of phosphorus after the crystallization. With this technique, the concentration of the catalytic element in the crystalline semiconductor film can be reduced to 1×10^{17} atoms/cm^3 or less, preferably to 1×10^{16} atoms/cm^3.

[0175]

The structure of this embodiment can be combined freely with all of the structures of Embodiments 1 through 10.

[0176]

[Embodiment 13]

This embodiment describes another mode of the gettering step with phosphorus which is shown in Embodiment 12. The basic process follows Fig. 1 and hence differences are picked out and explained.

[0177]

First, the state of Fig. 3D is obtained by following the process of Embodiment 1. Fig. 14A shows a state in which the resist masks 324 to 327 are removed from the state of Fig.

shown in Embodiment 10 is used and the catalytic element used is removed from the crystalline semiconductor film. To remove the catalytic element, this embodiment employs the technique disclosed in Japanese Patent Application Laid-open No. Hei 10-270363 (corresponding to US. Patent Application No. 09/050,182).

[0174]

It is the technique described in the publication to remove a catalytic element used in crystallization of an amorphous semiconductor film by utilizing the gettering effect of phosphorus after the crystallization. With this technique, the concentration of the catalytic element in the crystalline semiconductor film can be reduced to 1×10^{17} atoms/cm^3 or less, preferably to 1×10^{16} atoms/cm^3.

[0175]

The structure of this embodiment can be combined freely with all of the structures of Embodiments 1 through 10.

[0176]

[Embodiment 13]

This embodiment describes another mode of the gettering step with phosphorus which is shown in Embodiment 12. The basic process follows Fig. 1 and hence differences are picked out and explained.

[0177]

First, the state of Fig. 3D is obtained by following the process of Embodiment 1. Fig. 14A shows a state in which the resist masks 324 to 327 are removed from the state of Fig.

3D. A semiconductor layer to become an active layer of TFT is formed by using a technique of the thermal crystallization shown in Embodiment 10.

[0178]

At this point, the source region 328 of the NTFT and the drain region 329 thereof, and the source region 331 of the PTFT and the drain region 332 thereof contain phosphorus in a concentration of 1×10^{19} to 1×10^{21} atoms/cm^3 (preferably 5×10^{20} atoms/cm^3).

[0179]

In this state, a heat treatment step is conducted in a nitrogen atmosphere at 500 to 800°C for 1 to 24 hours, for example, at 600°C for 12 hours, in this embodiment. Through the step, the doped impurity elements that give n type and p type can be activated. Further, the catalytic element (nickel in this embodiment) remained after the crystallization step moves in the direction of the arrow and is gettered (trapped) by the above-mentioned action of phosphorus included in the source regions and drain regions. As a result, the nickel concentration in the channel formation region can be reduced to 1×10^{17} atoms/cm^3 or less.

[0180]

Once the process of Fig. 14B is completed, subsequent processes are conducted in accordance with the processes of Embodiment 1 to manufacture the CMOS circuit shown in Fig. 3E. Needless to say, similar processes are performed in the pixel matrix circuit.

[0181]

The structure of this embodiment can be combined freely with all of the structures of Embodiments 1 through 10.

[0182]

[Embodiment 14]

The TFT structure of the present invention can be applied not only to electro-optical devices such as AM-LCDs but also to every kind of semiconductor circuit. It may be applied to microprocessors such as RISC processors and ASIC processors, to signal processing circuits such as D/A converters, and to high frequency circuits for portable equipment (cellular phones including PHS, and mobile computers).

[0183]

Further, it is possible to obtain a semiconductor device with a three-dimensional structure in which an interlayer insulating film is formed on a conventional MOSFET and the present invention is applied to form a semiconductor circuit thereon. The present invention thus is applicable to all of the semiconductor devices that currently employ LSIs. That is, the present invention may be applied to the SOI structure (a TFT structure using a single crystal semiconductor thin film) such as SIMOX, Smart-Cut (trade name of SOITEC), and ELTRAN (trade name of Canon, Inc.).

[0184]

The semiconductor circuits of this embodiment can be realized by using a structure obtained from any combination of Embodiments 1, 2 and 4 through 13.

[0185]

[Embodiment 15]

A CMOS circuit and pixel matrix circuit formed by carrying out the present invention can be applied to various electro-optical devices and semiconductor circuits. That is, the present invention is applicable to all of electronic devices that incorporate those electro-optical devices and semiconductor circuits as components.

[0186]

Given as such electronic devices are video cameras, digital cameras, projectors, projection TVs, head mounted displays (goggle type displays), automobile navigation systems, personal computers, portable information terminals (mobile computers, cellular phones, electronic books or the like), etc. Examples of those are shown in Fig. 15.

[0187]

Fig. 15A shows a cellular phone, which is composed of a main body 2001, an audio output unit 2002, an audio input unit 2003, a display device 2004, operation switches 2005, and an antenna 2006. The present invention is applicable to the audio output unit 2002, the audio input unit 2003, the display device 2004, and other signal controlling circuits.

[0188]

Fig. 15B shows a video camera, which is composed of a main body 2101, a display device 2102, an audio input unit 2103, operation switches 2104, a battery 2105, and an image receiving unit 2106. The present invention is applicable to

the display device 2102, the audio input unit 2103, and other signal controlling circuits.

[0189]

Fig. 15C shows a mobile computer, which is composed of a main body 2201, a camera unit 2202, an image receiving unit 2203, operation switches 2204, and a display device 2205. The present invention is applicable to the display device 2205 and other signal controlling circuits.

[0190]

Fig. 15D shows a goggle type display, which is composed of a main body 2301, display devices 2302, and arm units 2303. The present invention is applicable to the display devices 2302 and other signal controlling circuits.

[0191]

Fig. 15E shows a rear projector, which is composed of a main body 2401, a light source 2402, a display device 2403, a polarization beam splitter 2404, reflectors 2405 and 2406, and a screen 2407. The present invention is applicable to the display device 2403 and other signal controlling circuits.

[0192]

Fig. 15F shows a front projector, which is composed of a main body 2501, a light source 2502, a display device 2503, an optical system 2504, and a screen 2505. The present invention is applicable to the display device 2502 and other signal controlling circuits.

[0193]

As described above, the applicable range of the present

invention is so wide that it can be applied to electronic devices in every field. The electronic devices of this embodiment can be realized by using a structure obtained from any combination of Embodiments 1 through 14.

[0194]

[Effect of the Invention]

The present invention is characterized in that the same NTFT can be used as both the GOLD structure and the LDD structure by controlling the voltage of a first wiring line provided under an active layer. In other words, the GOLD structure and the LDD structure can be formed on the same substrate without increasing the number of processes or complicating the process.

[0195]

Therefore, in the semiconductor device such as an AM-LCD and electronic device that has the AM-LCD as a display, circuits with optimal functions can be arranged in accordance with the specifications required for the circuits, thus greatly improving the performance and reliability of the semiconductor device.

[BRIEF DESCRIPTION OF THE INVENTION]

[Fig. 1] shows a structure of a CMOS circuit.

[Fig. 2] shows a structure of a pixel matrix circuit.

[Fig. 3] shows a process of manufacturing a CMOS circuit.

[Fig. 4] shows a process of manufacturing a pixel matrix circuit.

[Fig. 5] shows a process of manufacturing a pixel matrix

circuit.

[Fig. 6] shows the outside appearance of AM-LCD.

[Fig. 7] shows a block structure of AM-LCD.

[Fig. 8] shows a structure of a CMOS circuit or a pixel matrix circuit.

[Fig. 9] shows a structure of a pixel matrix circuit (specially a storage capacitor).

[Fig. 10] shows a structure of a CMOS circuit or a pixel matrix circuit.

[Fig. 11] shows a structure of a CMOS circuit or a pixel matrix circuit.

[Fig. 12] shows a process of manufacturing a CMOS circuit.

[Fig. 13] shows a structure of a CMOS circuit.

[Fig. 14] shows a process of manufacturing a CMOS circuit.

[Fig. 15] shows an example of an electronic device.